Curriculum Vitae

Jinwoo Kim

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Research Interests

Design and analysis of 2.5D/3D ICs, Analog and mixed signal IC design.

Education

Ph.D	**Georgia Institute of Technology**, Atlanta, GA, United States Electrical and Computer Engineering	Aug. 2017 – Present
M.S.	**Seoul National University,** Seoul, Republic of Korea Electrical Engineering and Computer Science *Thesis: "Power Clock Generator Using an Active Inductor for Charge Recovery Logic*"	Mar. 2011 – Feb. 2013
B.S.	**Seoul National University,** Seoul, Republic of Korea Electrical and Computer Engineering	Mar. 2003 – Feb. 2011

Publications

Journal

- Jinwoo Kim, Bon Woong Ku, Junsik Yoon, and Sung Kyu Lim, "An Effective Block Pin Assignment Approach for Block-level Monolithic 3D ICs," IEEE Journal of Exploratory Solid-State Computational Devices and Circuits.
- Jinwoo Kim, Venkata Chaitanya Krishna Chekuri, Nael Mizanur Rahman, Majid Ahadi Dolatsara, Hakki Mert Torun, Madhavan Swaminathan, Saibal Mukhopadhyay, and Sung Kyu Lim, "Chiplet/Interposer Co-Design for Power Delivery Network Optimization in Heterogeneous 2.5D ICs", IEEE Transactions on Components, Packaging and Manufacturing Technology.
- Edward Lee, Daehyun Kim, Jinwoo Kim, Sung Kyu Lim and Saibal Mukhopadhyay, "A ReRAM Memory Compiler for Monolithic-3D Integrated Circuits in a Carbon Nanotube Process," ACM Journal on Emerging Technologies in Computing Systems.
- Arjun Chaudhuri, Sanmitra Banerjee, Jinwoo Kim, Heechun Park, Bon Woong Ku, Sukeshawr Kannan, Krishnendu Chakrabarty and Sung Kyu Lim, "Built-in self-test and fault localization for inter-layer vias in monolithic 3D ICs", ACM Journal on Emerging Technologies in Computing Systems.
- Majid Ahadi Dolatsara, Jose Hejase, Wiren Dale Becker, Jinwoo Kim, Sung Kyu Lim, and Madhavan Swaminathan, "Worst-case Eye Analysis of High-speed Channels Based on Bayesian

Optimization," IEEE Transactions on Electromagnetic Compatibility. Vol. 63, No. 1, pp. 246-258, 2021.

- Heechun Park, Jinwoo Kim, Venkata Chaitanya Krishna Chekuri, Majid Ahadi Dolatsara, Mohammed Nabeel, Alabi Bojesomo, Satwik Patnaik, Ozgur Sinanoglu, Madhavan Swaminathan, Saibal Mukhopadhyay, Johann Knechtel, and Sung Kyu Lim, "Design Flow for Active Interposer-Based 2.5D ICs and Study of RISC-V Architecture with Secure NoC", IEEE Transactions on Components, Packaging and Manufacturing Technology, Vol. 10, No. 12, pp. 2047-2060, 2020.
- Jinwoo Kim, Gauthaman Murali, Heechun Park, Eric Qin, Hyoukjun Kwon, Venkata Chaitanya Krishna Chekuri, Nael Mizanur Rahman, Nihar Dasari, Arvind Singh, Minah Lee, Hakki Mert Torun, Kallol Roy, Madhavan Swaminathan, Saibal Mukhopadhyay, Tushar Krishna, and Sung Kyu Lim, "Architecture, Chip, and Package Co-design Flow for Interposer-based 2.5D Chiplet Integration Enabling Heterogeneous IP Reuse," IEEE Transactions on Very Large Scale Integration Systems. Vol. 28, No. 11, pp. 2424-2437, 2020.
- Arjun Chaudhuri, Sanmitra Banerjee, Heechun Park, Jinwoo Kim, Gauthaman Murali, Edward Lee, Daehyun Kim, Sung Kyu Lim, Saibal Mukhopadhyay, and Krishnendu Chakrabarty, "Advances in Design and Test of Monolithic 3D ICs," IEEE Design & Test. Vol. 37, No. 4, pp. 92-100, 2020.
- Minah Lee, Arvind Singh, Hakki M.Torun, Jinwoo Kim, Sung Kyu Lim, Madhavan Swaminathan, and Saibal Mukhopadhyay, "Automated I/O Library Generation for Interposer-based System-in-Package Integration of Multiple Heterogeneous Dies," IEEE Transactions on Components, Packaging, and Manufacturing Technology. Vol. 10, No. 1, pp. 111-122, 2020.

Conference

- Sanmitra Banerjee, Arjun Chaudhuri, Jinwoo Kim, Gauthaman Murali, Marc Nelson, Sung Kyu Lim, and Krishnendu Chakrabarty, "ParaMitE: Mitigating parasitic CNFETs in the presence of unetched CNTs", IEEE International Conference on Computer-Aided Design, 2021.
- Anthony Agnesina, Moritz Brunion, Jinwoo Kim, Alberto Garcia-Ortiz, Dragomir Milojevic, Francky Catthoor, Manu Perumkunnil and Sung Kyu Lim, "Power, Performance, Area and Cost Analysis of Memory-on-Logic Face-to-Face Bonded 3D Processor Designs", ACM/IEEE International Symposium on Low Power Electronics and Design, 2021.
- Jinwoo Kim, Lingjun Zhu, Hakki Mert Torun, Madhavan Swaminathan, and Sung Kyu Lim, "Micro-bumping, Hybrid Bonding, or Monolithic? A PPA Comparative Study for Emerging Heterogeneous 3D Integration Options", ACM Design Automation Conference (DAC), 2021.
- Jinwoo Kim, Venkata Chaitanya Krishna Chekuri, Nael Mizanur Rahman, Majid Ahadi Dolatsara, Hakki Torun, Madhavan Swaminathan, Saibal Mukhopadhyay and Sung Kyu Lim, “Silicon vs. Organic Interposer: PPA and Reliability Tradeoffs in Heterogeneous 2.5D Chiplet Integration,” IEEE International Conference on Computer Design (ICCD), 2020.
- Jinwoo Kim, Gauthaman Murali, Pruek Vanna-iampikul, Edward Lee, Daehyun Kim, Arjun Chaudhuri, Sanmitra Banerjee, Krishnendu Chakrabarty, Saibal Mukhopadhyay, Sung Kyu Lim, “RTL-to-GDS Design Tools for Monolithic 3D ICs," IEEE International Conference on Computer-Aided Design (ICCAD), 2020.
- Victor Huang, Da Eun Shim, Jinwoo Kim, Sai Pentapati, Sung Kyu Lim, and Azad Naeemi, "Modeling and Benchmarking Back End Of The Line Technologies on Circuit Designs at Advanced Nodes," IEEE International Interconnect Technology Conference, 2020.
- Jinwoo Kim, Heechun Park, Edward Lee, Daehyun Kim, Arjun Chaudhuri, Sanmitra Banerjee, Mark Nelson, Krishnendu Chakrabarty, Saibal Mukhopadhyay, and Sung Kyu Lim, "RTL-to-GDS Design Tools for Monolithic 3D ICs Built with Carbon Nanotube Transistors and Resistive Memory," Government Microcircuit Applications and Critical Technology (GOMACTech), 2020.
- Hakki Torun, Huan Yu, Nihar Dasari, Venkata Chaitanya Krishna Chekuri, Arvind Singh, Jinwoo Kim, Sung Kyu Lim, Saibal Mukhopadhyay and Madhavan Swaminathan, "A Spectral

Convolutional Net for Co-Optimization of Integrated Voltage Regulators and Embedded Inductors," IEEE International Conference on Computer-Aided Design (ICCAD), 2019.

- Heechun Park, Kyungwook Chang, Bon Woong Ku, Jinwoo Kim, Edward Lee, Daehyun Kim, Arjun Chaudhuri, Sanmitra Banerjee, Saibal Mukhopadhyay, Krishnendu Chakrabarty, and Sung Kyu Lim, "RTL-to-GDS Tool Flow and Design-for-Test Solutions for Monolithic 3D ICs," ACM Design Automation Conference (DAC), 2019. (Invited Paper)
- Jinwoo Kim, Gauthaman Murali, Heechun Park, Eric Qin, Hyoukjun Kwon, Venkata Chaitanya Krishna Chekuri, Nihar Dasari, Arvind Singh, Minah Lee, Hakki Mert Torun, Kallol Roy, Madhavan Swaminathan, Saibal Mukhopadhyay, Tushar Krishna and Sung Kyu Lim, "Architecture, Chip, and Package Co-design Flow for 2.5D Integration of Reusable IP Chiplets", ACM Design Automation Conference (DAC), 2019.
- Jinwoo Kim, Eric Qin, Heechun Park, Tushar Krishna, and Sung Kyu Lim, "Enabling Heterogeneous IP Reuse with Interposer-based 2.5D ICs and Custom Interface Protocol," Government Microcircuit Application and Critical Technology Conference (GOMACTech), 2019.
- Minah Lee, Arvind Singh, Hakki Mert Torun, Jinwoo Kim, Sung Kyu Lim, Madhavan Swaminathan, and Saibal Mukhopadhyay, "Automated Generation of All-Digital I/O Library Cells for Multiple Dies in System-in-Package Integration," Government Microcircuit Application and Critical Technology Conference (GOMACTech), 2019.
- Hakki Mert Torun, Nihar Dasari, Arvind Singh, Minah Lee, Jinwoo Kim, Heechun Park, Hyouk Joon Kwon, Eric Qin, Tushar Krishna, Sung Kyu Lim, Saibal Mukhopadhyay, and Madhavan Swaminathan, "Design Space Exploration of Power Delivery in Heterogeneous Integration," Government Microcircuit Application and Critical Technology Conference (GOMACTech), 2019.
- Minah Lee, Arvind Singh, Hakki Mert Torun, Jinwoo Kim, Sung Kyu Lim, Madhavan Swaminathan, and Saibal Mukhopadhyay, "Automated Generation of All-Digital IO Library Cells for System-in-Package Integration of Multiple Dies," IEEE Electrical Performance of Electronic Packaging and Systems (EPEPS), 2018.
- Minah Lee, Jinwoo Kim, Arvind Singh, Hakki Mert Torun, Madhavan Swaminathan, Sung Kyu Lim, and Saibal Mukhopadhyay, "On the Design of Energy-Efficient I/O Circuits for Interposer-based 2.5D System-in-Package," IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2018.
- Jinwoo Kim, Sunkwon Kim, Hyoungmin Lee, and Suhwan Kim "Power Clock Generator Using an Active Inductor," IEEK Fall Conference 2012, pp.45-49, Nov. 2012.
- Sungwon Yim, Hyoungmin Lee, Jinwoo Kim, and Suhwan Kim "Verilog-AMS Modeling of Flyback PFC Converter," IEEK Fall Conference 2011, pp.85-88, Nov. 2011.

Patents

- Jin-Woo Kim, Byeong-Taek Moon and Jun-Ho Kim, "Tag detector of near field communication (NFC) device, NFC device and mobile device including the same," US Patent 9,853,697.
- Jinwoo Kim, Junho Kim, Seok-Hyun Kim and Hangseok Choi, "Wireless communication device and method of operating the same," US Patent 9,722,672.
- Jun-Ho Kim, Young-Joo Lee, Jong-Pil Cho and Jin-Woo Kim, "Demodulator for near field communication, near field communication device, and electronic device having the same," US Patent 9,634,729.
- Byeongtaek Moon, Jinwoo Kim and Junho Kim, "Data transceiver device and receiving method for near field communication," US Patent 9,571,168.

Research Experience

Graduate Research Assistant Aug. 2017 – Present
GTCAD Laboratory, Georgia Institute of Technology, Atlanta, GA, United States
Advisor: Prof. Sung Kyu Lim
Research Interests: Design and analysis of 2.5D/3D ICs

Current Projects:
- **RTL-to-GDS Tools and Methodologies for Sequential Integration Monolithic 3D ICs (DARPA, 2018 – 22)**

Previous Projects:
- **A Vertically-Integrated Design Flow for IP Reuse and Heterogeneous Integration (DARPA, 2017 – 21)**

Graduate Research Assistant Mar. 2011 – Feb. 2013
AMiC Laboratory, Seoul National University, Seoul, Republic of Korea
Advisor: Prof. Suhwan Kim
Research Interests: Charge-recovery circuitry design

- **Power clock generator design for charge recovery circuitry**
  - Design power clock generator using an active inductor for the area reduction
  - Implemented in 65nm technology
- **LED driver design**
  - Fly-back PFC converter design to achieve high efficiency

Visiting Student Dec. 2011 – Jul. 2012
University of Michigan, Ann Arbor, MI, United States
Research Interests: Charge-recovery circuitry design

- **Subthreshold Boost Logic (SBL), a dual-rail charge-recovery logic family**
  - Power clock generator design in TSMC 65nm
  - BIST (Built-In Self-Test) design in TSMC 65nm

Work Experience

Technical Intern Apr. 2021 – Aug. 2021
Synopsys Inc., Mountain View, CA, United States

- **3D IC Compiler**

Engineer Feb. 2013 – Jul. 2017
Samsung Electronics Co., Ltd., Hwaseong, Republic of Korea
Security Product Development Team, S.LSI division
Display Solution Development Team, S.LSI division

- **Near Field Communication IC**
  - Designed RF front-end for Samsung Galaxy smartphone series
    - NFC receiver for NFC reader/writer mode in 45nm tech.
    - NFC tag detector for low power operation of NFC reader/writer mode in 45nm tech.
  - Designed Magnetic Secure Transmission(MST) IC for Samsung Pay
- **Panel display driver IC**
  - Designed source driver IC for QUHD/UHD/FHD LCD panels
  - Support USI-T, mini-LVDS, CMPI interfaces

Honors and Awards

Best Paper Award Oct. 21st 2020
The 38th IEEE International Conference on Computer Design (ICCD), 2020.
Hartford, Connecticut, USA (Virtual)

Skills

EDA Tools
- Synopsys Design Compiler, Cadence Innovus, Cadence Tempus, Cadence Voltus, Virtuoso, HSPICE, Spectre, Calibre, NC-Verilog, ModelSim, Xilinx ISE

Languages
- Verilog, C, C++, Perl, Tcl, HSPICE, Python